A High-Efficiency 94-GHz 0.15-μm InGaAs/InAlAs/InP Monolithic Power HEMT Amplifier

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***Abstract*—We report high efficiency W-band power monolithic microwave integrated circuits (MMIC's) using passivated 0.15 μm gate length $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As/InP$ HEMT's. A 0.15 μm $\times$ 320 μm single stage InP power HEMT MMIC amplifier demonstrates a maximum power added efficiency of 23% with 40 mW output power and 4.9 dB power gain at 94 GHz. When biased for higher output power, 54 mW output power with 20% power added efficiency was achieved at 94 GHz. These results represent the best combination of efficiency and output power fixtured data reported to date at this frequency.**

I. Introduction

HIGH EFFICIENCY solid-state power amplifiers at W-band represent a critical component for many future weapons systems applications including smart munitions and advanced phased arrays. Although GaAs-based HEMT's have demonstrated good performance up to 60 GHz, it suffers from lower device gain at 94 GHz and higher frequencies which have limited the device and monolithic microwave integrated circuit (MMIC) output power and power-added efficiencies (PAE's). Lattice-matched $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As/InP$ HEMT's (InP HEMT's) have higher gain, higher cutoff frequency, lower source resistance, higher maximum current densities and higher substrate thermal conductivity compared to GaAs-based HEMT's [1]–[4]. These advantages are translated to higher device PAE and output power at W-band. Most of the previously reported work at W-band are based on pseudomorphic GaAs-based HEMT technology and the best reported data for GaAs-based HEMT's at W-band was a 160 μm device with 13% PAE and 63 mW output power [5]–[8]. In this letter, we report the fixture measured results of a high-efficiency 94-GHz 0.15 μm$\times$ 320 μm monolithic single-stage InP power HEMT amplifier with a maximum PAE of 23% with 40 mW output power when biased for highest efficiency. When biased for highest output power, 54 mW output power was achieved with 20% PAE. To the best of our knowledge, this is the first reported InP-based power MMIC's at W-band measured in fixture, and these results represent the highest combination of PAE and output power reported to date at this frequency.

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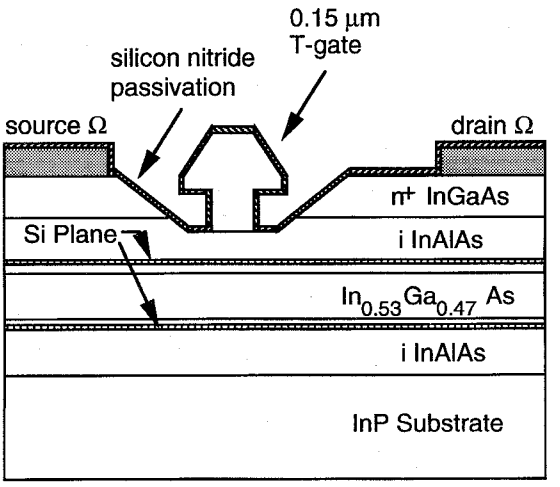

Fig. 1. Layer structure of a double heterostructure passivated 0.15 μm $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As/InP$ power HEMT.

II. Device Design

The double doped, double heterostructure lattice-matched InP HEMT (shown in Fig. 1) is grown using molecular beam epitaxy on a 2-in InP substrate. Two silicon doping planes are employed on the upper and lower InAlAs layers to achieve a high channel sheet concentration. Typical room temperature and 77K Hall mobilities of 9000 and 30 000, respectively, with a sheet carrier concentration of 4.0×10^{12} cm^{-2} are measured. The design of a thick n^+ InGaAs cap layer and InAlAs layer are optimized to simultaneously achieve low source resistance, high cutoff frequency at high bias, and high breakdown. These features are all crucial to achieve high device power added efficiency at 94 GHz. Another key device design is a compact device layout, which reduces device parasitic capacitances and resistances, decreases the input and output combining losses, and shortens the source airbridge and reduces the series feedback inductance for the 94-GHz multifinger devices. The compact structure is further aided by a reduction in substrate thickness from 3 mil to 2 mil, which reduces the size of the source vias. The 2-mil substrate thickness also significantly improves thermal conductivity and device source inductance.

The 0.15 μm gate length device is passivated with 500-Å-thick silicon nitride and a liftoff silicon nitride process is used

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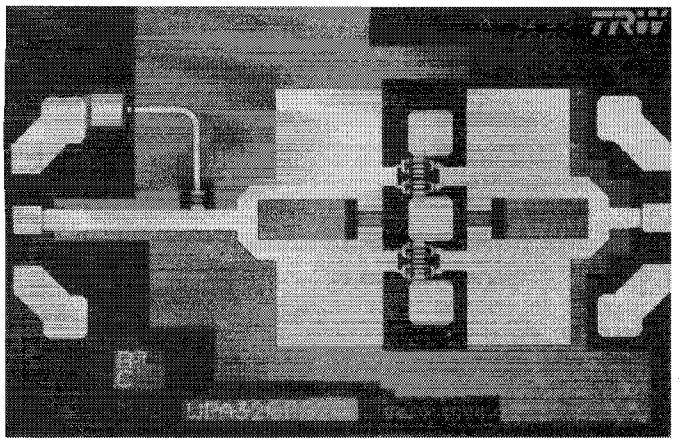

Fig. 2. Diagram of a single-stage MMIC 94-GHz 0.15 μm x 320 μm InP HEMT power amplifier.

to define the MIM capacitors used in the single-stage power amplifier designs. The wafers are thinned to 2 mil (50 μm and wet-etched ground via holes are defined with a typical diameter of 60 μm for very low device source inductance; 3-μm backside gold metal is plated and the wafers are diced for chip fixture testing.

III. Device and Amplifier Results

The 0.15-μm InP HEMT has demonstrated transconductances (G_m) greater than 800 mS/mm, maximum current density ($I_{\max}$) greater than 550 mA/mm, cutoff frequencies (f_T) greater than 140 GHz, and maximum available gain greater than 10 dB at a drain bias of 2 V. The high device f_T and gain achieved is important for high PAE, especially for 94-GHz power operation. Gate to drain breakdowns greater than 5 V at 0.1 mA/mm gate current have been achieved.

Linear and nonlinear device models for 0.15 μm gate length eight-finger 160 μm gate width devices have been derived from measured device I-V characteristics and small-signal S-parameters up to 50 GHz. Based on these models, single-stage monolithic 94-GHz amplifiers were designed by paralleling two of the 160-μm unit cells (320 μm total gate width) between three source via holes. The input and output were matched to 50 Ω using quasi-low-pass matching networks. The overall size of the circuit (shown in Fig. 2) is 1.0 mm x 0.8 mm. The diced chips were mounted into a W-band (WR-10) waveguide fixture with 0.8 dB loss per finline transition. Gate and drain dc biases were applied from off-chip bias networks fabricated as part of the transition on the fused silica substrate. The off-chip bias networks consist of a quarter wavelength high impedance line and a radial stub for RF grounding. The power characteristics of the measured device are shown in Fig. 3 (corrected for losses). The single stage MMIC exhibited 23% PAE with 40 mW (16 dBm) output power and 4.9 dB gain when biased for the best PAE (V_d = 2 V, I_d = 58 mA). When biased for higher output power (V_d = 2.5 V, I_d = 68.1 mA), 54 mW (17.3 dBm) output power with 20% PAE with 4.3 dB gain was measured. No tuning or tweaking was performed to achieve better performance. In Fig. 4, PAE

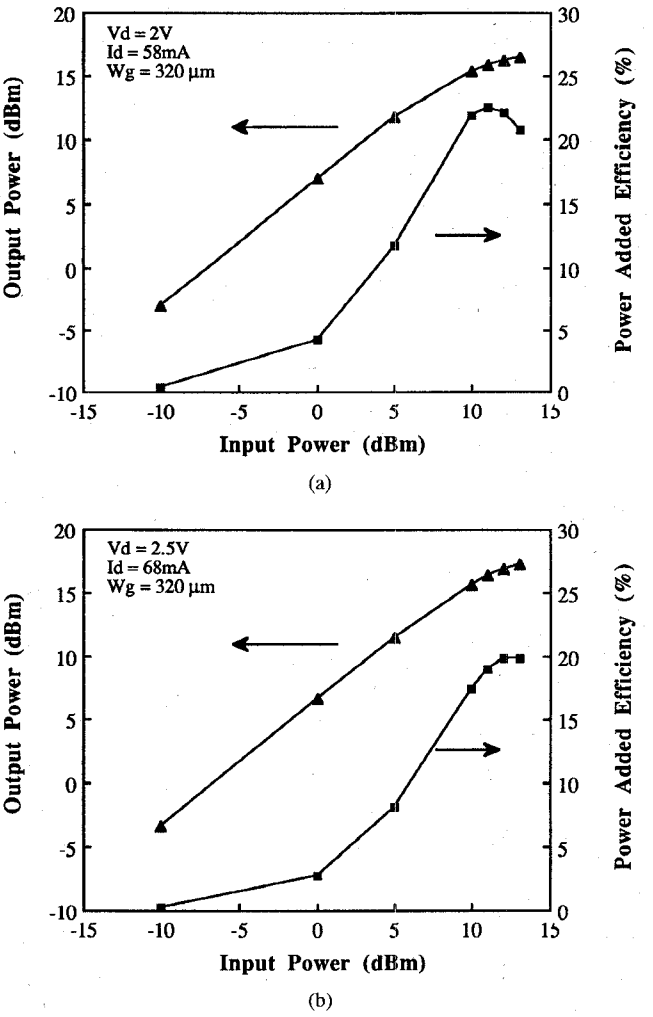

Fig. 3. Measured output power and PAE of a 94-GHz 320-μm gate width single-stage InP HEMT power amplifier biased for (a) highest PAE (V_d = 2 V, I_d = 58 mA) and (b) highest P_{out} (V_d = 2.5 V, I_d = 68 mA).

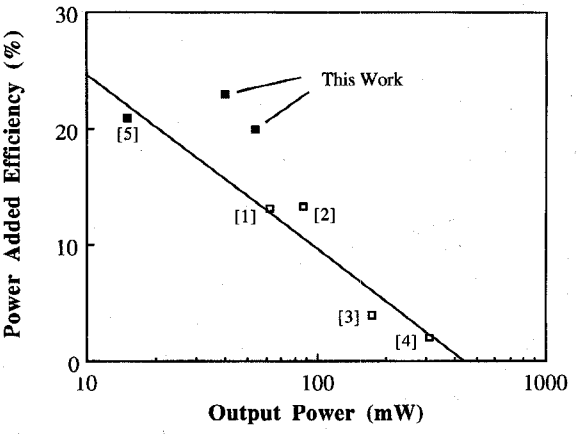

Fig. 4. Reported fixtured W-band HEMT PAE versus output power performance comparing previously reported GaAs-based PHEMT results and InP-based HEMT results from this letter.

versus output power at W-band is plotted, comparing the results achieved in this letter against the best-reported W-band power HEMT results that have been measured in fixture [1]–[5]. The plot demonstrates the superior combination of PAE and output power achieved on these InP-based HEMT's MMIC's compared to GaAs-based PHEMT's.

The major limitation to the maximum drain operating voltage and ultimately the output power capability of the InP HEMT device is due to low drain to source breakdown, which is believed to be due to impact ionization in the channel previously reported by several authors [9], [10]. Future improvements in device breakdown and device gain through device structure and process optimizations should result in higher device power added efficiencies and output power at 94 GHz.

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